

Appl. No. 09/634,706
Amdt. dated Aug 18, 2004
Reply to Office Action of May 20, 2004

Amendments to Specification:

Please replace the paragraph containing lines 2 to 10 with the following paragraph:

-- According to the present invention there is provided an inverse multiplexer device comprising an input port for receiving a stream of data packets, a plurality of output ports for connection to outgoing physical links, a transmit buffers for preparing outgoing packets, an expansion port capable of receiving packets from said buffers and transferring them through a corresponding expansion port ~~capable of receiving packets from said buffers and transferring them through a corresponding expansion port on another like inverse multiplexer to designated output links on the other inverse multiplexer, and a controller for outputting the data packets on a group of any of said links in accordance with an inverse multiplex protocol, whereby said multiplexers can be cascaded to increase the number of output links that can be accommodated~~ for transfer to said output ports, a first expansion port capable of receiving packets from said transmit buffers and transferring them through a corresponding second expansion port on an other like inverse multiplexer device to designated outgoing physical links on said other inverse multiplexer device; and a controller for transferring the data packets in a round-robin fashion from said transmit buffers through said output ports or said expansion port to a group of outgoing physical links made up of links associated with both said inverse multiplexer device and said other inverse multiplexer device and forming an inverse multiplex group in accordance with an inverse multiplex protocol whereby said inverse multiplexer devices can be cascaded to increase the number of output links that can be accommodated by said inverse multiplex protocol. --

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Please replace the paragraph containing lines 4 to 6 on page 5 with the following paragraph:

-- The RAM controller 48 is connected to RAM 56, rate recovery block 58, RX scheduler 60 and UTOPIA interface 62. This interface outputs are a stream of ATM cells corresponding to the input stream. --

Please replace the paragraph containing lines 12 to 17 on page 6 with the following paragraph:

-- Bytes coming off the ring 30 are received in ring receiver 90 and passed to address comparator 92, wherein they are compared with addresses stored in ring address register 94. If an incoming message contains a byte intended for the device, it is output from the comparator 92 either as a transmit byte Tx or a receive byte Rx. If it is a transmit byte Tx, it is passed to the appropriate output port 22. If it is a receive byte Rx, it is passed to the appropriate cell delineation block 42 of the receive portion of the device. --